3D FDTD Analysis of a SOT353 Package Containing a Bipolar Wideband Cascode Transistor Using the Compression Approach

M. Rittweger♣, M. Werthen♣, J. Kunisch♣, I. Wolff♣, FELLOW, IEEE, P. Chall♦, B. Balm♦, and P. Lok♦

♣Institut für Mobil- und Satellitenfunktechnik
Moerser Str. 316, D-47475 Kamp-Lintfort, FRG

♦Philips Semiconductors B.V.
Gerstweg 2, 6534 AE Nijmegen, The Netherlands

Abstract

A 3d electromagnetic simulation of an entire mold injected plastic package including its coplanar environment is presented. The active elements are substituted by inner ports. The resulting network is connected with measured transistor data using a circuit simulator. A comparison of the simulated data with measured results is shown. The influence of the package and therefore the meaning of such a simulation procedure is discussed.

Introduction

Mold injected plastic packages, as a standard solution for integrated circuit packaging are used for frequencies up to a few GHz. The fabrication process is that of a typical mass product and therefore hardly to prepare in laboratory scale. Therefore electromagnetic simulation is an important tool for package design [1]. Especially FDTD analysis in combination with the compression method is able to predict the performance of the packaged device [2].

SOT353 Device Simulation

Fig. 1 shows the outline of the SOT353 package investigated in our paper. It is a typical surface mounted device with 5 pins and a 0805 size (.08"×.05").

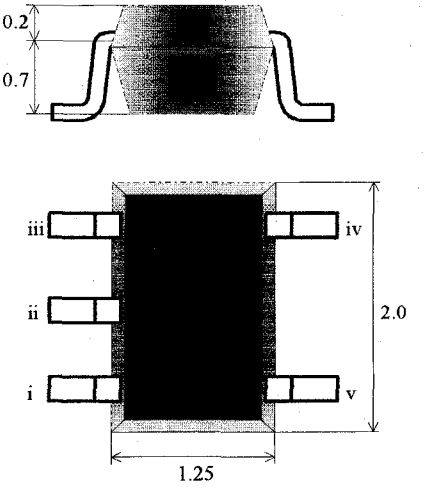

Fig. 1: Package outline (top view, mm).

It contains two NPN bipolar transistors in a cascode configuration (Fig. 2).

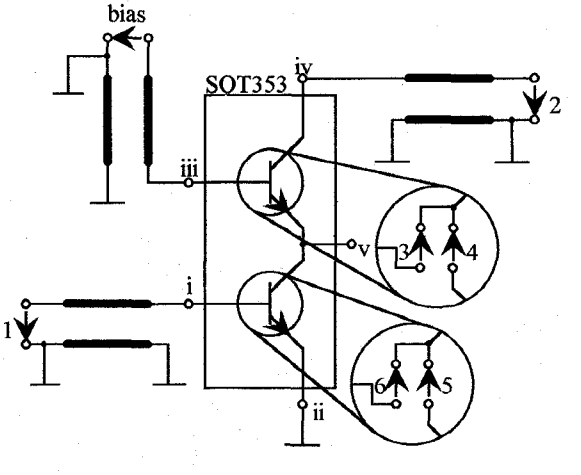

Fig. 2: The circuit with coplanar (1, 2) and inner ports (3-6).

TH 4C

The discrete crystals are mounted directly with their collector on the leadframe. Base and emitter are connected using bond wires. The cascode amplifier BFC505 is primarily intended for low power RF communications equipment and has very low feedback capacitance resulting in high isolation. The layout of the leadframe and the coplanar environment, the package is soldered on, is shown in Fig. 3. Port 1 (pin i) and port 2 (pin iv) are input and output of the amplifier, respectively. A third transmission line (pin iii) is used for well defined broadband biasing with matched termination (specs are defined for RF-ground at pin iii). Pin ii is grounded and pin v is not connected. Ports 3 up to 6 are inner ports to substitute the transistor's function. These ports are restricted to one electric field node connecting the bond wire to the lead frame. They are described by voltage and current. Formal Heaviside transformations are used to determine wave quantities:

$$\underline{a}_n = \frac{1}{2}\left(\frac{\underline{u}_n}{\sqrt{Z_{cn}}} + \underline{i}_n\sqrt{Z_{cn}}\right), \quad (1a)$$

$$\underline{b}_n = \frac{1}{2}\left(\frac{\underline{u}_n}{\sqrt{Z_{cn}}} - \underline{i}_n\sqrt{Z_{cn}}\right). \quad (1b)$$

So by varying the terminations the basic field and current distributions, describing the passive structure can be achieved. Table 1 contains terminations (reflection coefficients) and excitations (incident waves) for six linear independent cases necessary to solve the linear equation to achieve S-parameters:

$$\mathbf{S} = \mathbf{B} \cdot \mathbf{A}^{-1}. \quad (2)$$

To provide linear independence each transmission line has to be excited at least one time. Furthermore each inner port termination has to be varied at least one time whereby the port quantities must not vanish for both variations.
The only restriction of the resulting S-matrix (or compression matrix) is that there are no wave effects within the ports (extension 50µm) and the current distribution in the transistors is described in a global manner. It has been verified in former publications [3] that there is no difference between this procedure called the compression method and a direct field simulation including the elements connected to the inner ports here. But the description of the passive environment is now available for small and large signal, multitone excitation and noise analysis.

number	port 1	port 2	port 3	port 4	port 5	port 6
1	0, a_{11}	0	-1	-1	-1	-1
2	0, a_{12}	0	1	-1	1	-1
3	0, a_{13}	0	1	1	1	-1
4	0	0, a_{24}	1	-1	1	1
5	0	0, a_{25}	-1	1	1	1
6	0	0, a_{26}	1	-1	-1	1

Table 1: Linear independent excitation.

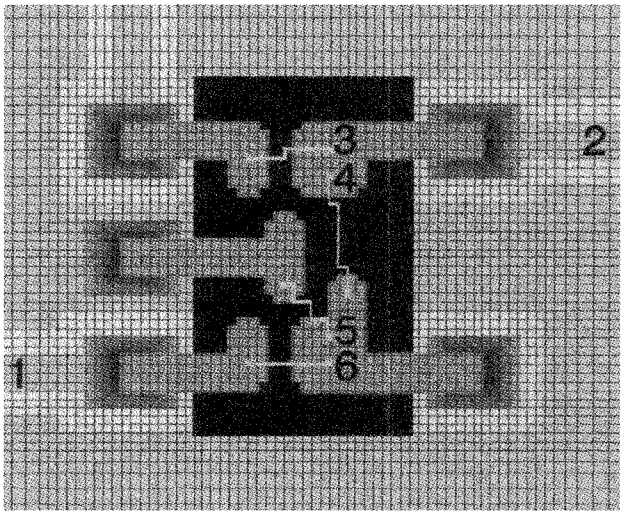

Fig. 3: Discretized structure with inner ports.

The inner ports should be used in such a way as to ensure that current flow is comparable to that of the physical device to achieve the best model [4, 5]. The cascode configuration shows a specific example for a port group [3] representing each transistor. Connections between inner ports of different groups lead to unphysical results because such a connection e.g. circumvents restrictions due to signal propagation delay.
Fig. 4 shows the 3d model generated using the simulators input data. The structure has been adapted to the orthogonal grid but is very similar to the real device.

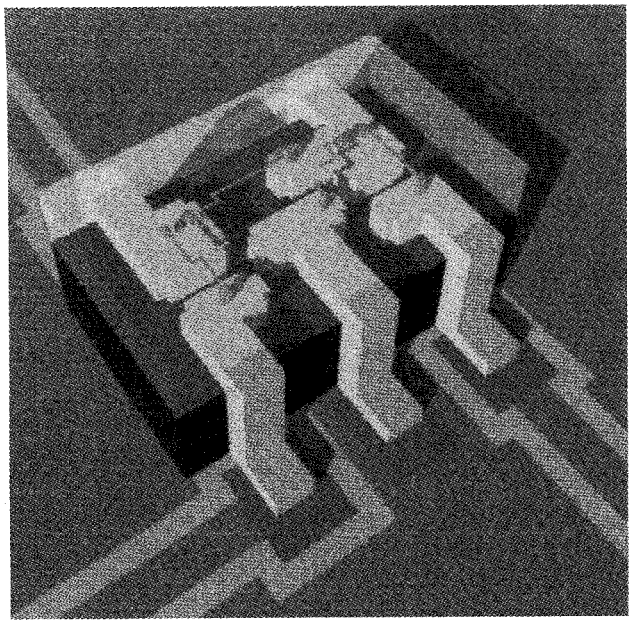

Fig. 4: 3d model of the package (transparent top).

Embedding of the Inner Circuits

The six-port scattering matrix of the passive structure (see Fig. 5) is now the data base for the connection with the transistor crystals.

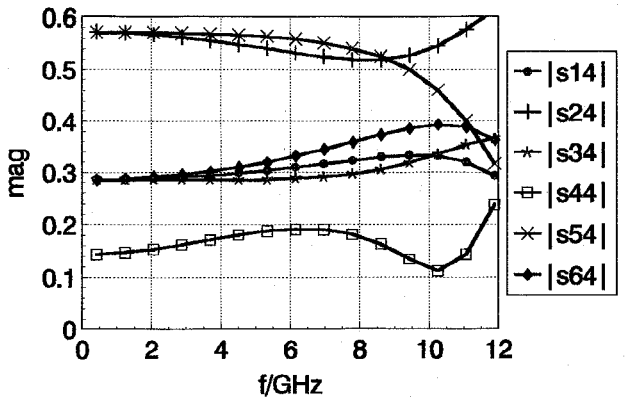

Fig. 5: Selected S-parameters of the package.

The inner transistor data has been achieved using measured results and a de embedding procedure based on the knowledge of a well known much simpler package. Since the inner ports are not related to ground, ideal transformers are used to connect the transistors as shown in Fig. 6.

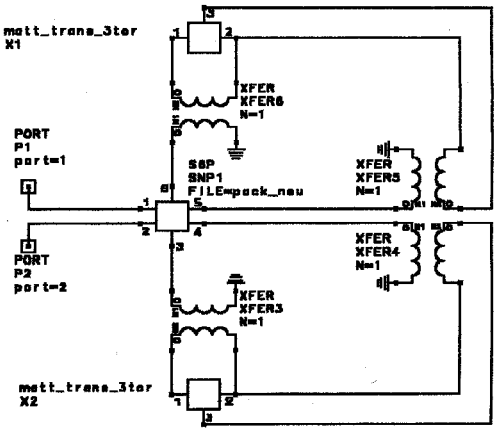

Fig. 6: Embedding of the transistors (HP-EEsof Libra).

Results

The structure was measured on a coplanar probe station and the comparison of measured (nwa) and simulated (fdtd) results is shown in Fig. 7 and 8. The curves labelled ideal show the S-parameters for an ideal circuitry without package effects. Since it is not possible to determine the correct phase shift in this case only absolute values of the S-parameters are shown. The authors took that choice of S-parameters, because here it can be seen clearly that the package's influence is not negligible.

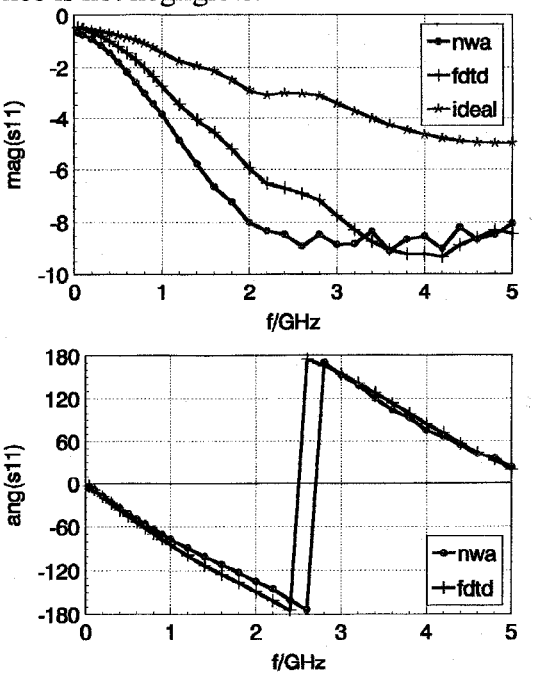

Fig. 7: Reflection coefficient of the amplifier's input.

The exact determination of the reflection coefficient at the input is necessary to achieve a correct impedance matching.

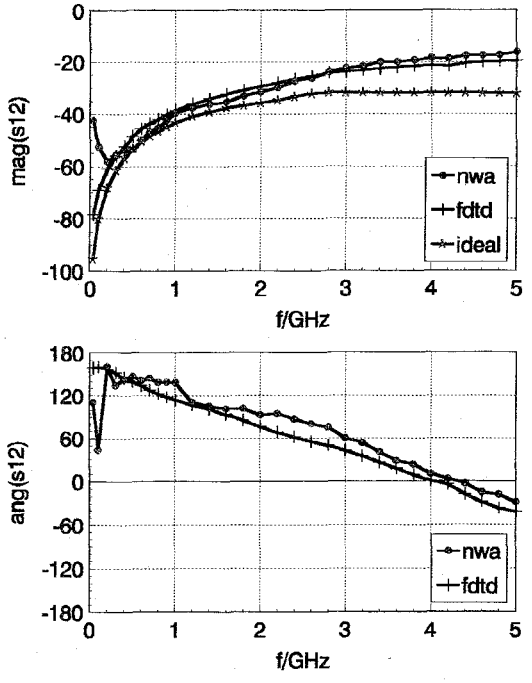

Fig. 8: Isolation of the amplifier.

The deviation between simulation and measurement for low frequencies is due to the non calibrated bias port. The bias tee has no good de coupling properties in this frequency range.
High isolation was a major goal for the design. So accurate package description is needed to reach the specs. The ideal circuitry (the curves labelled ideal in Fig. 7, 8) is not sufficient to predict the performance of the packaged device as it can be seen in the comparison above.

Summary

The performance of a packaged device has been predicted using an analysis procedure based on a 3D FDTD simulation. The package description in form of a network matrix can be used for large signal or noise analysis as well.

Acknowledgement

The authors wish to thank P. Uhlig for preparation of the test device, W. Lütke and B. Hopf for preparing the transistor data and measurements.

References

[1] P. Mezzanotte, M. Mongiardo, L. Roselli, and R. Sorrentino, "FDTD analysis of high performance MMIC package," *IEEE MTT-S Intern. Symp. Digest*, pp. 337-340, May 1994.

[2] J. Kunisch, M. Rittweger, S. Heinen, and I. Wolff, "The compression approach: a new technique for the analysis of distributed circuits containing nonlinear elements," *21st EuMC Proceedings*, Stuttgart, pp. 1296-1301, Sept. 1991.

[3] J. Kunisch, A. Bahr, M. Rittweger, and I. Wolff, "Analysis of nonlinear microwave circuits using the compression approach," *IEEE MTT-S Intern. Symp. Digest*, pp. 637-640, June 1993.

[4] M. Rittweger, M. Werthen, and I. Wolff, "FDTD simulation for microwave packages and interconnects," *IEEE MTT-S Workshop on EM Modeling of Microwave Packages and Interconnects Proceedings*, invited paper, (Atlanta), pp. 78-91, June 1993.

[5] T. Shibata and H. Kimura, "Computer aided engineering for microwave and millimeter-wave circuits using the FD-TD technique of field simulations," invited paper, *Int. J. Microwave and MM-Wave Comp.-Aided Eng.*, vol. 3, pp. 238-250, 1993.